AMENDMENTS

In the Specification:

Amend the paragraph beginning at page 10, line 25, as follows:

A selector 37 is a selection circuit. This circuit selects an error computation value from the first error computer 35 in the case where "1" is outputted by the comparator 24, and selects an error computation value from the second error computer 36 in a case where "0" is outputted. Then, the bi-level error computed at the bi-level error computing section [[35]] 25 is held at the error storage section 28 by three lines, and is weighted by the peripheral error weighting filter section 23 of 5 x 3 in matrix size. By a series of these circuits, a bi-level error is diffused, and density storage type area gradation is performed.